



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,130	02/28/2002	Nikki M. Bruner	P1569US01	4401

7590 07/21/2005

Fellers, Snider, Blankenship, Bailey & Tippens,
Bank One Tower
100 North Broadway,
Suite 1700
Oklahoma City, OK 73102-8820

EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 07/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,130	BRUNER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 01 July 2005.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-13 and 15-28 is/are pending in the application.
 4a) Of the above claim(s) 1-13 and 28 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 15-27 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 16 November 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

Election/Restrictions

1. Newly submitted claim 28 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claim 28 recites, "predicting error rate performance in relation to a selected digital data configuration", whereas claim 15 explicitly recites, "comparing the output data with the input data to determine an error rate performance". Claim 28 does not recite "comparing the output data with the input data to determine an error rate performance" and hence cannot be classified in 714/719 (Read-in and Read-out with compare) where claim 15 is classified. Claim 28 is directed to predicting error rate in relation to a selected digital data configuration and does not recite a comparison step. Since claim 28 recites no comparison step, claim 28 is properly classified in 714/780 (Forward Error Correction using Symbol Reliability).

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 28 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicant's election with traverse of group II (claims 15-27) in the reply filed on 07/01/2005 is acknowledged. The traversal is on the ground(s) that the Examiner misinterpreted the claim language of claim 1. This is not found persuasive because

claim 1 still does not recite, "comparing the output data with the input data to determine an error rate performance" and hence cannot be classified in 714/719 as claim 15 is.

The Applicant contends, "The claim phrase "predict error rate performance in relation to each configuration" plainly means in relation to the input and output data at the first configuration or in relation to the input and output data at the second configuration.

There simply is no basis for the Examiner's construction that it can mean in relation to the input at the first configuration and the output at the second configuration".

That is entirely incorrect. The phrase "predict error rate performance in relation to each configuration" plainly means what it says that error rate performance is predicted in relation to each configuration. That the input and output data can be characterized in at least two alternative digital configurations demonstrates no relationship whatsoever between predicting error rate and the input data and output data. Furthermore, nowhere does claim 1 recite, "comparing the output data with the input data to determine an error rate performance" and hence cannot be classified in 714/719 as claim 15 is.

The Applicant contends, "Although Applicant maintains the position that the Examiner's basis for the restriction requirement is erroneous, nevertheless the amendment to claim 1 herein is made solely to more particularly point out and distinctly claim the patentable subject matter of the present invention. Claim 1 as currently amended more particularly recites that the predicted error rate performance is in relation to a *first of the alternative digital configurations for both the input data and output data and, alternatively, to a second of the alternative digital configurations for both the input data and output data*".

The newly amended claim language suffers from the deficiencies of previously examined claim language. Claim 1 still only recites that error rate is predicted in relationship to alternative digital configurations. The examiner would like to point out that this means exactly what it says that error rate is predicted in relationship to alternative digital configurations. That the alternative digital configurations are used for the input data and output data in no way demonstrates that error rate is predicted in relationship to the input data and output data since the alternative digital configurations can be applied after the prediction is made without any knowledge of the input data and output data. Furthermore, nowhere does claim 1 recite, "comparing the output data with the input data to determine an error rate performance" and hence cannot be classified in 714/719 as claim 15 is.

Finally, the Examiner would like to point out that the primary purpose of restrictions is to reduce the burden of having to examine more than one invention. The Examiner asserts that claims 1-13 and 28 are different inventions that require entirely different searches and that there is no way the Examiner could be expected to do a thorough search and examination of all the pending claims. The Examiner asserts that, because of the broadness, a thorough search of claim 15 as written requires at least the following EAST search as a minimum <((recording adj medium) (storage adj device)) and (compare compares compared comparing comparator)>, which produces 167,035 Prior Art patent documents, which is already a burden for the Examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claims 1-13 and 28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 07/01/2005.

Claim Objections

2. Claim 15 is objected to because of the following informalities: Claim 15 recites "Method", in the preamble. As such it is impossible to determine to what the Applicant regards as his invention. The Examiner would like to point out that the Applicant's specification only teaches arranging the input data into a selected ECC and RLL configurations from a plurality of different selectable ECC and RLL configurations to predict error rate performance of different selectable ECC and RLL configurations. The Examiner asserts that that encryption codes, partial response codes, etc. are all digital configurations that the Applicant's disclosure is silent on. Furthermore, the Examiner asserts that claim 15 as written requires the following EAST search as a minimum <((recording adj medium) (storage adj device)) and (compare compares compared comparing comparator)>, which produces 167,035 Prior Art patent documents. The Examiner asserts that not only is such a search impossible, but the Applicant's specification does not warrant such a search since the Applicant's specification only teaches selectable RLL and ECC digital configurations for the purposes of predicting error rate performance of different ECC and RLL configurations. As such the Examiner has narrowed the current search and asserts that not only has the Examiner not

searched every conceivable interpretation of the claims (some of which have been pointed out, above), but that such a search is impossible.

The Examiner suggests that the Applicant rewrite the preamble to more clearly reflect what invention claims 15-27 are directed to and to clearly claim what the Applicant regards as his invention as required by 37 CFR 1.75.

Appropriate correction is required.

Claim 27 is objected to because of the following informalities: it is not clear whether claim 27 is intended to be an independent claim having the same limitations as claim 15 or whether claim 27 depends from claim 15. If claim 27 is meant to be independent, it should not refer to another claim. If claim 27 is dependant, then it must also be written as a method claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 15-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 15 recites "Method", in the preamble. As such it is impossible to

determine to what the Applicant regards as his invention. The Examiner would like to point out that the Applicant's specification only teaches arranging the input data into a selected ECC and RLL configurations from a plurality of different selectable ECC and RLL configurations to predict error rate performance of different selectable ECC and RLL configurations. The Examiner asserts that that encryption codes, partial response codes, etc. are all digital configurations that the Applicant's disclosure is silent on. That is, the Applicant fails to teach every conceivable interpretation for claim 15.

Furthermore, the Examiner asserts that claim 15 as written requires the following EAST search as a minimum <((recording adj medium) (storage adj device)) and (compare compares compared comparing comparator)>, which produces 167,035 Prior Art patent documents. The Examiner asserts that not only is such a search impossible, but the Applicant's specification does not warrant such a search since the Applicant's specification only teaches selectable RLL and ECC digital configurations for the purposes of predicting error rate performance of different ECC and RLL configurations. As such the Examiner has narrowed the current search and asserts that not only has the Examiner not searched every conceivable interpretation of the claims (some of which have been pointed out, above), but that such a search is impossible.

The Examiner suggests that the Applicant rewrite the preamble to more clearly reflect what invention claims 15-27 are directed to and to clearly claim what the Applicant regards as his invention or to explain where and how the specification teaches every conceivable interpretation for the claim language such as when the digital configurations are encryption codes, partial response codes, etc so as to enable one of ordinary skill in

the art at the time the invention was made to make and use the Applicant's claimed invention.

Claim 1 recites, "arranging the input data into a selected digital configuration from a plurality of different selectable digital configurations".

The Examiner would like to point out that the Applicant's specification only teaches arranging the input data into a selected ECC and RLL configurations from a plurality of different selectable ECC and RLL configurations to predict error rate performance of different selectable ECC and RLL configurations. The Examiner asserts that that encryption codes, partial response codes, etc. are all digital configurations that the Applicant's disclosure is silent on. That is, the Applicant fails to teach every conceivable interpretation for claim 15.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 15-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites, "the comparing step is characterized by using a first error correction code (ECC) encoding methodology based on the selected digital configuration". The terms "characterized by" and "based on" are indefinite since 1) it is not clear what the relationship between "the comparing step" and a "first error correction code (ECC)

encoding methodology" is, and 2) it is not clear what the relationship between a "first error correction code (ECC) encoding methodology" and "the selected digital configuration" is.

Claim 17 recites, "the comparing step is characterized by determining a number of errors in the output data in relation to a selected number of errors that can be detected by the first error correction code (ECC) encoding methodology". The terms "characterized by" and "in relation to" are indefinite since 1) it is not clear what the relationship between "the comparing step" and a "determining a number of errors" is, and 2) it is not clear what the relationship between a "determining a number of errors" and "a selected number of errors that can be detected" is.

Claim 18 recites, "the arranging the input and output data steps are characterized by sequences of multibit symbols each having a selected symbol length". The term "characterized by" is indefinite since it is not clear what the relationship between "the arranging the input and output data steps" and a "sequences of multibit symbols" is.

Claim 19 recites, "the arranging the input and output data steps are characterized by sequences of multibit symbols each having a second selected symbol length". The term "characterized by" is indefinite since it is not clear what the relationship between "the arranging the input and output data steps" and a "sequences of multibit symbols" is.

Claim 20 recites, "the comparing step is characterized by predicting error rate performance using a second error correction code (ECC) encoding methodology based on the second selected symbol length". The terms "characterized by" and "based on" are indefinite since 1) it is not clear what the relationship between "the comparing step"

and a “predicting error rate performance” is, and 2) it is not clear what the relationship between a “predicting error rate performance” and “the second selected symbol length” is.

Claim 21 recites, “the arranging the input and output data steps are characterized by performing run length limited (RLL) encoding upon the input data and inhibiting RLL decoding of the output data to reflect said RLL encoding”. The terms “characterized by” and “to reflect” are indefinite since it is not clear what the relationship between “the arranging the input and output data steps” and a “performing run length limited (RLL) encoding” is.

In addition, It is not clear what is meant by “to reflect said RLL encoding”. Does the applicant mean –depending on whether the output is RLL encoded or not--?

Claim 22 recites, “the arranging the input and output data steps are characterized by arranging the data into a plurality of interleaves”. The term “characterized by” is indefinite since it is not clear what the relationship between “the arranging the input and output data steps” and a “arranging the data into a plurality of interleaves” is.

Claim 23 recites, “concurrently inhibiting and emulating selected operations of the digital data channel”. It is not clear what the “selected operations” have to do with any of the elements in claim 15. Claim 23 is indefinite.

Claim 24 recites, “the comparing step is characterized by predicting the error rate in relation to only one selected digital configuration of the input and output data”. The terms “characterized by” and “in relation to” are indefinite since 1) it is not clear what the relationship between “the comparing step” and a “predicting the error rate” is, and 2)

it is not clear what the relationship between a “predicting the error rate” and “only one selected digital configuration” is.

Claim 25 recites, “the comparing step is characterized by predicting the error rate in relation to two or more selected digital configurations of the input and output data”.

The terms “characterized by” and “in relation to” are indefinite since 1) it is not clear what the relationship between “the comparing step” and a “predicting the error rate” is, and 2) it is not clear what the relationship between a “predicting the error rate” and “two or more selected digital configurations of the input and output data” is.

Claim 26 recites, “the comparing step is characterized by predicting the error rate in relation to differences between the input sequence and the output sequence”. The terms “characterized by” and “in relation to” are indefinite since 1) it is not clear what the relationship between “the comparing step” and a “predicting the error rate” is, and 2) it is not clear what the relationship between a “predicting the error rate” and “differences between the input sequence and the output sequence” is.

Claim 27 recites, “A disc drive comprising a digital data channel configured in accordance with the method of claim 15”. The term “configured in accordance with” is indefinite since it is not clear what the relationship between the method and hardware elements of a “disc drive comprising a digital data channel” is. In addition, it is not clear whether claim 27 is intended to be an independent apparatus claim or whether it is intended to be dependant upon a method claim. If it is intended to be independent, it comprises only a preamble with no body and, if it is intended to be dependant, it fails to further limit the method of claim 15 by providing an additional step.

Claims 15-27 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. Claim 16 recites, “the comparing step is characterized by using a first error correction code (ECC) encoding methodology based on the selected digital configuration”. The omitted elements are as follows: the relationship between “the comparing step” and a “first error correction code (ECC) encoding methodology”, and 2) the relationship between a “first error correction code (ECC) encoding methodology” and “the selected digital configuration”.

Claim 17 recites, “the comparing step is characterized by determining a number of errors in the output data in relation to a selected number of errors that can be detected by the first error correction code (ECC) encoding methodology”. The omitted elements are as follows: the relationship between “the comparing step” and a “determining a number of errors”, and 2) the relationship between a “determining a number of errors” and “a selected number of errors that can be detected”.

Claim 18 recites, “the arranging the input and output data steps are characterized by sequences of multibit symbols each having a selected symbol length”. The omitted elements are as follows: the relationship between “the arranging the input and output data steps” and a “sequences of multibit symbols”.

Claim 19 recites, “the arranging the input and output data steps are characterized by sequences of multibit symbols each having a second selected symbol length”. The

omitted elements are as follows: the relationship between “the arranging the input and output data steps” and a “sequences of multibit symbols”.

Claim 20 recites, “the comparing step is characterized by predicting error rate performance using a second error correction code (ECC) encoding methodology based on the second selected symbol length”. The omitted elements are as follows: the relationship between “the comparing step” and a “predicting error rate performance”, and 2) the relationship between a “predicting error rate performance” and “the second selected symbol length”.

Claim 21 recites, “the arranging the input and output data steps are characterized by performing run length limited (RLL) encoding upon the input data and inhibiting RLL decoding of the output data to reflect said RLL encoding”. The omitted elements are as follows: the relationship between “the arranging the input and output data steps” and a “performing run length limited (RLL) encoding”.

Claim 22 recites, “the arranging the input and output data steps are characterized by arranging the data into a plurality of interleaves”. The omitted elements are as follows: the relationship between “the arranging the input and output data steps” and a “arranging the data into a plurality of interleaves”.

Claim 23 recites, “concurrently inhibiting and emulating selected operations of the digital data channel”. The omitted elements are as follows: the relationship between the “selected operations” and any of the elements in claim 15.

Claim 24 recites, “the comparing step is characterized by predicting the error rate in relation to only one selected digital configuration of the input and output data”. The

omitted elements are as follows: the relationship between “the comparing step” and a “predicting the error rate”, and 2) the relationship between a “predicting the error rate” and “only one selected digital configuration of the input and output data”.

Claim 25 recites, “the comparing step is characterized by predicting the error rate in relation to two or more selected digital configurations of the input and output data”.

The omitted elements are as follows: the relationship between “the comparing step” and a “predicting the error rate”, and 2) the relationship between a “predicting the error rate” and “two or more selected digital configurations of the input and output data”.

Claim 26 recites, “the comparing step is characterized by predicting the error rate in relation to differences between the input sequence and the output sequence”. The omitted elements are as follows: the relationship between “the comparing step” and a “predicting the error rate”, and 2) the relationship between a “predicting the error rate” and “differences between the input sequence and the output sequence”.

Claims 15-27 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. Claim 16 recites, “the comparing step is characterized by using a first error correction code (ECC) encoding methodology based on the selected digital configuration”. The omitted steps are: the steps for characterizing “the comparing step” using a “first error correction code (ECC) encoding methodology”, and 2) the steps for using a “first error correction code (ECC) encoding methodology” based on “the selected digital configuration”. That is, steps linking “the comparing step”, “first error

correction code (ECC) encoding methodology" and "the selected digital configuration" are missing.

Claim 17 recites, "the comparing step is characterized by determining a number of errors in the output data in relation to a selected number of errors that can be detected by the first error correction code (ECC) encoding methodology". The omitted steps are: the steps for characterizing "the comparing step" using a "determining a number of errors", and 2) the steps for "determining a number of errors" in relation to "a selected number of errors that can be detected". That is, steps linking "the comparing step", "determining a number of errors" and "a selected number of errors that can be detected" are missing.

Claim 18 recites, "the arranging the input and output data steps are characterized by sequences of multibit symbols each having a selected symbol length". The omitted steps are: the steps for characterizing "the arranging the input and output data steps" using a "sequences of multibit symbols".

Claim 19 recites, "the arranging the input and output data steps are characterized by sequences of multibit symbols each having a second selected symbol length". The omitted steps are: the steps for characterizing "the arranging the input and output data steps" using a "sequences of multibit symbols".

Claim 20 recites, "the comparing step is characterized by predicting error rate performance using a second error correction code (ECC) encoding methodology based on the second selected symbol length". The omitted steps are: the steps for characterizing "the comparing step" using a "predicting error rate performance", and 2)

the steps for using a “predicting error rate performance” based on “the second selected symbol length”. That is, steps linking “the comparing step”, “predicting error rate performance” and “the second selected symbol length” are missing.

Claim 21 recites, “the arranging the input and output data steps are characterized by performing run length limited (RLL) encoding upon the input data and inhibiting RLL decoding of the output data to reflect said RLL encoding”. The omitted steps are: the steps for characterizing “the arranging the input and output data steps” using a “performing run length limited (RLL) encoding”.

Claim 22 recites, “the arranging the input and output data steps are characterized by arranging the data into a plurality of interleaves”. The omitted steps are: the steps for characterizing “the arranging the input and output data steps” using a “arranging the data into a plurality of interleaves”.

Claim 23 recites, “concurrently inhibiting and emulating selected operations of the digital data channel”. The omitted steps are as follows: the steps relating the “selected operations” to any of the elements in claim 15.

Claim 24 recites, “the comparing step is characterized by predicting the error rate in relation to only one selected digital configuration of the input and output data”. The omitted steps are: the steps for characterizing “the comparing step” using a “predicting the error rate”, and 2) the steps for “predicting the error rate” in relation to “only one selected digital configuration of the input and output data”. That is, steps linking “the comparing step”, “predicting the error rate” and “only one selected digital configuration of the input and output data” are missing.

Claim 25 recites, “the comparing step is characterized by predicting the error rate in relation to two or more selected digital configurations of the input and output data”.

The omitted steps are: the steps for characterizing “the comparing step” using a “predicting the error rate”, and 2) the steps for “predicting the error rate” in relation to “two or more selected digital configurations of the input and output data”. That is, steps linking “the comparing step”, “predicting the error rate” and “two or more selected digital configurations of the input and output data” are missing.

Claim 26 recites, “the comparing step is characterized by predicting the error rate in relation to differences between the input sequence and the output sequence”. The omitted steps are: the steps for characterizing “the comparing step” using a “predicting the error rate”, and 2) the steps for “predicting the error rate” in relation to “differences between the input sequence and the output sequence”. That is, steps linking “the comparing step”, “predicting the error rate” and “differences between the input sequence and the output sequence” are missing.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 15-20 and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shikakura; Akihiro (US 5687182 A).

35 U.S.C. 102(b) rejection of claim 15.

Shikakura teaches using a digital data channel to store input data to a data storage medium (see Figure 4 in Shikakura; Note: The Authoritative Dictionary of IEEE Standards Terms defines channel as a path along which signals can be sent; hence a storage medium along with its read, write and recovery circuitry is a channel); subsequently using the digital data channel to obtain output data from the medium (Data Reproduction Unit 32 in Figure 4 in Shikakura is a channel component used to obtain output data from the medium); arranging the input data into a selected digital configuration from a plurality of different selectable digital configurations (col. 2, lines 29-34 in Shikakura teaches a selectable means for selecting different error correction codes with different error correction capabilities; different selectable error correction codes with different error correction capabilities are different selectable digital configurations); arranging the output data into the selected digital configuration (col. 2, lines 29-34 in Shikakura teaches that the input data as well as the output data is arranged into the selected digital configuration so that the selected digital configured error correction code can be decoded to remove errors); and comparing the output data with the input data to determine an error rate performance (col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original input data after encoding

and prior to being passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero).

35 U.S.C. 102(b) rejection of claim 16.

Col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original input data after encoding and prior to being passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero.

35 U.S.C. 102(b) rejection of claim 17.

Col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original

input data after encoding and prior to being passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero. Note: syndromes are used to generate error locations and magnitudes for the number of errors found.

35 U.S.C. 102(b) rejection of claim 18.

ECC parity or redundancy is a symbol having a selected symbol length. A word train is also a sequence of symbols, each symbol being a word. See Abstract in Shikakura.

35 U.S.C. 102(b) rejection of claim 19.

Col. 2, lines 24-26 in Shikakura teaches that different code rates are used for different ECC codes; hence the ratio of data to ECC parity or redundancy changes, that is, the ECC symbol for different code rates is different.

35 U.S.C. 102(b) rejection of claim 20.

Col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration for whatever ECC code is being used at the time; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original input data after encoding and prior to being

passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero.

35 U.S.C. 102(b) rejection of claim 24.

Col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration for whatever ECC code is being used at the time; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original input data after encoding and prior to being passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero.

35 U.S.C. 102(b) rejection of claim 25.

Col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration for whatever ECC code is being used at the time; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original input data after encoding and prior to being

passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero.

35 U.S.C. 102(b) rejection of claim 26.

Col. 3, lines 11-29 in Shikakura teaches that syndromes are generated and used to count the number of errors within a predetermined time duration for whatever ECC code is being used at the time; Note: error rate is defined as the number of errors within a predetermined time duration; Note also: that a syndrome for an error correction code is 0, if the output data is equal to the original input data after encoding and prior to being passed through the storage medium, and is non-zero, if the output data is not equal to the input data; hence a syndrome is substantially a comparison result indicating that the output data matches the input data when the syndrome is zero and indicating that the output data does not match the input data when the syndrome is not zero.

35 U.S.C. 102(b) rejection of claim 27.

Claim 27 fails to add any meaningful limitation to claim 27 since it recites no additional method step.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shikakura; Akihiro (US 5687182 A) in view of Reed; David E. et al. (US 6115198 A, hereafter referred to as Reed).

35 U.S.C. 103(a) rejection of claims 21.

Shikakura substantially teaches the claimed invention described in claims 15-20, 23 and 24 (as rejected above).

However Shikakura does not explicitly teach the specific use of RLL code.

Reed, in an analogous art, teaches use of RLL code (see RLL Encoder 6 in Figure 2 of Reed).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shikakura with the teachings of Reed by including use of RLL code. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of RLL code would have provided the opportunity to minimize errors caused by non-linear transition shift.

35 U.S.C. 103(a) rejection of claim 22.

Shikakura substantially teaches the claimed invention described in claims 15-20 (as rejected above).

However Shikakura does not explicitly teach the specific use of interleaving.

Reed, in an analogous art, teaches use of interleaving (see Interleaver 100 in Figure 9A of Reed).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schachner with the teachings of Reed by including use of interleaving. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of interleaving would have provided the opportunity to effectively decode RLL encoded data.

7. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shikakura; Akihiro (US 5687182 A) in view of Schachner; Joseph M. et al. (US 6442730 B1, hereafter referred to as Schachner).

35 U.S.C. 103(a) rejection of claim 23.

Shikakura substantially teaches the claimed invention described in claims 15-20 (as rejected above).

However Shikakura does not explicitly teach the specific use of concurrently inhibiting and emulating selected operations of the digital data channel.

Schachner, in an analogous art, teaches emulation (col. 23, lines 35-42 in Schachner teach an emulation mode for channel emulation).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Shikakura with the teachings of Schachner by including use of emulation. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of emulation would have provided failure analysis capabilities (see Abstract in Schachner).

However Schachner does not explicitly teach the specific use of inhibiting selected operations of the digital circuit block.

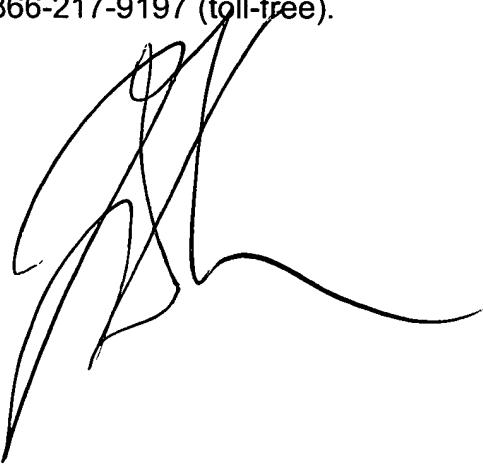
The Examiner asserts that the error analysis during emulation is based upon channel emulation, hence it would be obvious to disable the actual channel to prevent channel data from interfering with error analysis.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Schachner by including use of inhibiting selected operations of the digital circuit block. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of inhibiting selected operations of the digital circuit block would have provided the opportunity to prevent channel data from interfering with error analysis.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133